ANALOG DEVICES

AN-27
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Polarity Programmable Peak Detector

Four ICs are used in this design to give positive or negative peak detection and reset levels over a ±10V range. A precision voltage comparator, a sample-and-hold amplifier, an open-collector exclusive-OR gate package, and a quad analog switch used as two SPDT switches are the principal components required.

BLOCK DIAGRAM

Figure 1 shows the basic circuit and the 4 modes of operation. A comparator continuously examines the difference between the present analog input voltage and a voltage peak held by the sample and hold (S/H) amplifier. If the present value exceeds the held value, the S/H is placed in the "Track" condition and acquires a new peak value returning to a "Hold" condition when coincidence is reached. The comparator's output is inverted or non-inverted depending on the polarity selected by POS/$\overline{\text{NEG}}$ SELECT. This same TTL control signal connects the appropriate voltage-programmed reset voltage to the S/H input during the RESET modes. In RESET the S/H is forced to a "Track" condition by the PEAK DETECT/$\overline{\text{RESET}}$ SELECT digital input. Figure 2 shows typical waveforms.

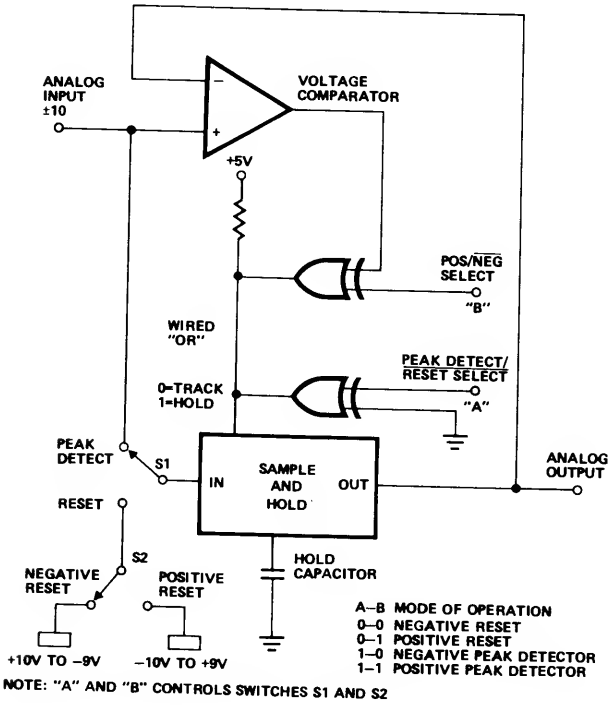

Figure 1. Programmable Peak Detector Block Diagram

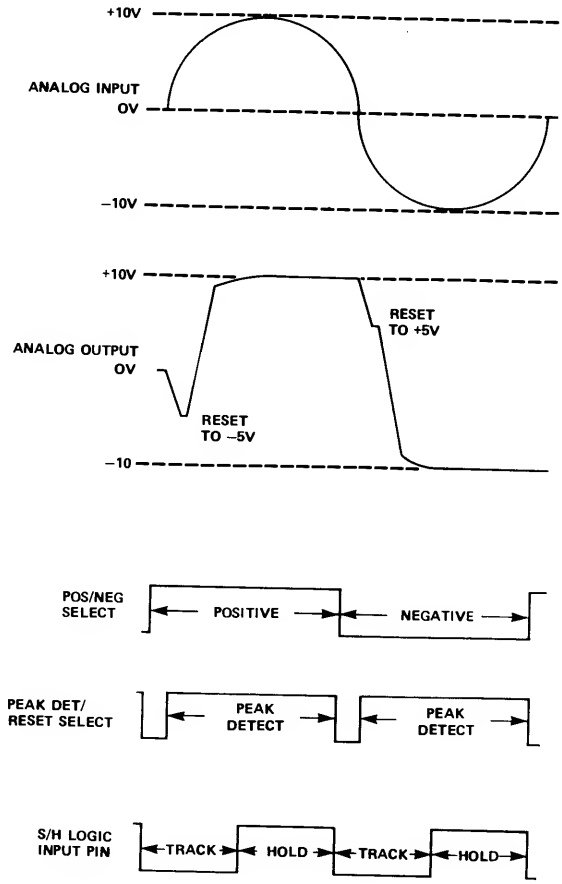

Figure 2. Programmable Peak Detector Waveforms

DETAILED CIRCUIT DESCRIPTION

In Figure 3, the SMP-11FY S/H is specified for three reasons: low cost, 2.5mV (Maximum) zero-scale error, and its 10V/μs slew rate. Together with the CMP-01CJ precision voltage comparator, system unadjusted DC accuracy is within 5mV at zero-scale and 10mV at full-scale. Comparator input overvoltage protection resistors and diodes are required as shown.

A SW-01 Quad Analog Switch connected at 2 SPDT switches connects the proper analog inputs to the S/H during the 4 modes of operation. 200 ohm current-limiting resistors are used as recommended by the switch manufacturer. Logic drive to the switch is provided by 1/2 of a SN74LS136 quad exclusive-OR gate used as 2 inverters.

Bypassing as shown is strongly recommended — 0.1μF ceramic dieletric capacitors for the comparator and the S/H, plus 10μF solid tantalum bypass capacitors physically close to the S/H. In addition the use of a ground plane is recommended to minimize ground path resistances. A 0.01μF hold capacitor is used to minimize overshoot when tracking high frequency analog inputs.

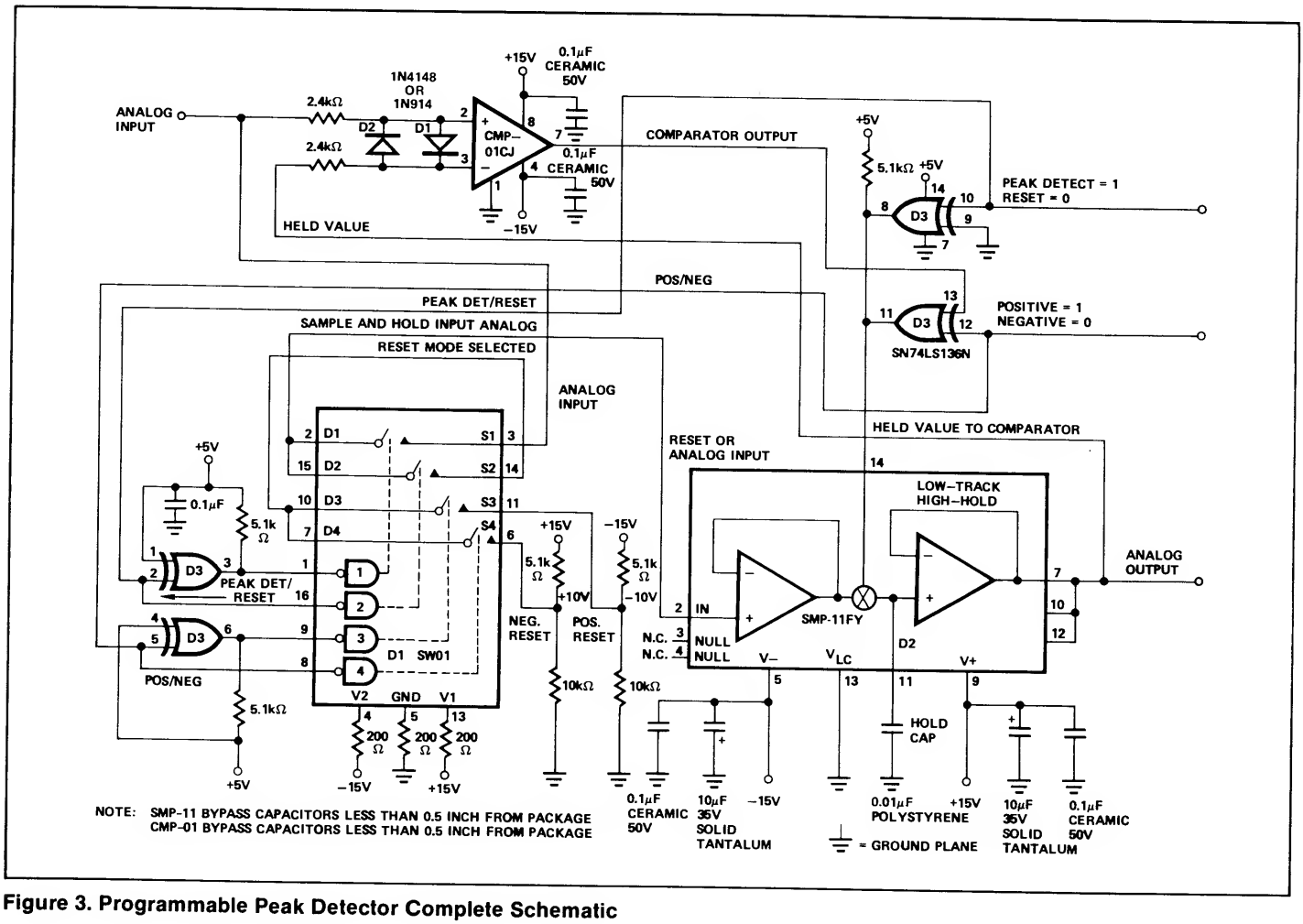

Figure 3. Programmable Peak Detector Complete Schematic